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Integrated High Step-Up Converter with WCCIS and VMCS for PV applications

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ABSTRACT

One of the most efficient and promising ways to solve the effect of conventional energy sources on the environment is to use Photovoltaic (PV) solar energy due to the clean, efficient, and environmentally friendly performance. A high step-up and high-efficiency dc–dc converter is necessary due to the relatively low output voltage of the PV arrays. These requirements make necessary the use of an interleaved boost converter with winding cross coupled inductors (WCCIs) and voltage multiplier cells (VMCs). The voltage gain is extended and the switch voltage stress is reduced by the WCCIs and the VMCs in the offered circuit, which reduces the peak current ripple of the power devices and makes low-voltage MOSFETs with high performance available in high step-up and high output voltage applications. Moreover, the out- put diode reverse-recovery problem is alleviated by the leakage inductance of the Winding-cross-coupled inductor, which decreases the reverse-recovery damages. Furthermore, the leakage energy is recycled by the voltage multiplier cells, when the switch turns off. In this paper detailed operating principles and steady state analysis are described. A 1 kW prototype with 40V input and 404 V output operating at 50 kHz switching frequency is built and tested to verify the significant improvements of the proposed converter.

KEY WORDS: PV cells, high step-up, interleaved boost converter, voltage multiplier cell, winding-cross-coupled inductor.

1. INTRODUCTION

In the past century, global surface temperatures have increased because the global warming is taking place due to effluent gas emissions and increase in CO2. The effect of conventional energy sources on the environment and the world's proved reserves of the oil, the coal and the natural gas could not satisfy the growing of the global energy demand. Along with the declining production of the fossil fuels, more and more researchers concentrate on exploring the renewable energy sources, such as the photovoltaic (PV) sources, the fuel cells, and the wind energy and so on. Among them, PV sources are predicted to become the biggest energy candidates by year 2040 due to the clean, efficient, and environmentally outgoing performance (Maycock 2006, Li and Wolfs 2008).

The energy produced from solar cells should have high efficiency, less loss. Hence a high step-up and high-efficiency dc–dc converter is necessary due to the relatively low output voltage of the PV arrays. Therefore the most important criteria under research are to have a high-efficiency DC–DC converter with high-voltage gain due to increasing demands. Commonly, the conventional boost converter cannot realize such a high voltage gain even with an extreme duty cycle due to the parasitic parameters limitation (Erickson and Maksimovic, 2001). The high voltage gain can be achieved by the cascade boost converter (Huber and Jovanovic, 2000), but the circuit is complex and the cost is high due to the cascade structure.

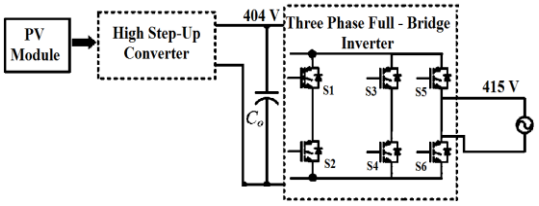

Figure.1.Three-phase PV grid-connected power system

A lot of single-stage high step-up and high-efficiency converters are explored by employing the coupled inductor recently (Zhao and Lee 2003, Tseng and Liang 2004, Wai and Duan 2005; Wu, 2005). The voltage gain is extended and the switch voltage stress is reduced by the transformer function of the coupled inductor. The leakage energy is recycled by the clamp circuit and the output diode reverse-recovery problem is alleviated by the leakage inductance. Unfortunately, the power level is limited and the input current ripple is large due to the single- phase operation.

The interleaved boost converters with switched capacitors are presented in (Giral, 2000; Prudente, 2008) for high step-up and high power applications. However, more switched capacitor cells are required to realize an extreme high voltage gain. A family of interleaved high step-up boost converters with winding-cross-coupled inductors (WCCIs) is proposed in (Li and He, 2008). The second and the third windings of the WCCIs serve as the dc voltage sources and are in series to the circuit to achieve a high step-up conversion and to reduce the switch voltage stress. The active clamp scheme is applied to recycle the leakage energy and to suppress the volt- age spikes in (Li and He 2007). However, one set of active clamp circuit and an additional gate driver are necessary for each phase, which in-

creases the circuit complexity. With some topology variations, the passive lossless clamp scheme can be derived to recycle the leakage energy and to suppress the turn-off voltage ringing on the MOSFETs.

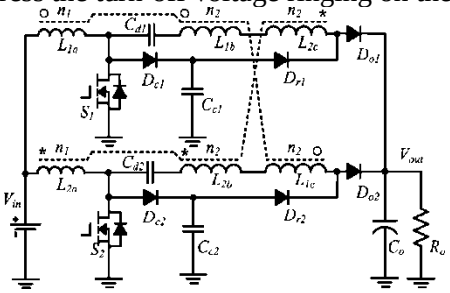

Figure.2. Proposed interleaved high step-up converter

A novel interleaved high step-up converter integrated with WCCIs and voltage multiplier cells is proposed in this paper. The voltage gain is prolonged and the switch voltage stress is reduced by the WCCIs and the voltage multiplier cells. ZCS turn-on soft switching performance is realized and the output diode reverse-recovery problem is alleviated by the leakage inductance of the WCCIs. The leakage energy is recovered and the turn- off voltage spikes are absorbed by the voltage multiplier cells. Furthermore, the voltage multiplier cells are inserted into the power branch to reduce the conduction losses and to extend the voltage gain compared with the circuit introduced in (Li and He, 2007). Simulation results of a 1 kW 40 V input and 400 V output prototypes operating at 50 kHz switching frequency with the significant improvements of the proposed converter is shown.

2. METHODS MATERIALS USED IN THE PROPOSED HIGH STEP - UP CONVERTER

The proposed interleaved high step-up converter is shown in Fig. 4. There are two coupled inductors in the circuit. Each coupled inductor has three windings and the third winding of the coupled inductor is inserted into another phase, which is named as WCCIs (Li and He 2008). The second winding with n_2 turns couples to the inductor in its phase with n_1 turns (L_{1b} versus L_{1a} & L_{2b} versus L_{2a}) and the third winding with n_2 turns couples to the inductors in another phase (L_{1c} versus L_{1a} and L_{1b}, L_{2c} versus L_{2a} and L_{2b}). The coupling reference of the WCCIs is marked by " ° " and " $*$ " as shown in Fig. 2. Each phase has one set of voltage multiplier cell (Giral et al. 2000), which is composed of a clamp diode $D_{c1}(D_{c2})$, a clamp capacitor $C_{c1}(C_{c2})$, a regenerative diode $D_{r1}(D_{r2})$ and a series capacitor $C_{d1}(C_{d2})$.

The features of the proposed method are: that it avoids the extreme duty cycle that exist in conventional interleaved boost converter because the voltage gain of the proposed converter is extended, the conduction loss is less due to the reduced duty cycle, the turn ratio is also less when compared to the conventional method that is and the efficiency is increased as the voltage stress is reduced, the output diode reverse-recovery problem is alleviated by the leakage inductance of the WCCI, which reduces the reverse-recovery losses. Furthermore, the leakage energy is recycled by the voltage multiplier cells, when the switch turns off.

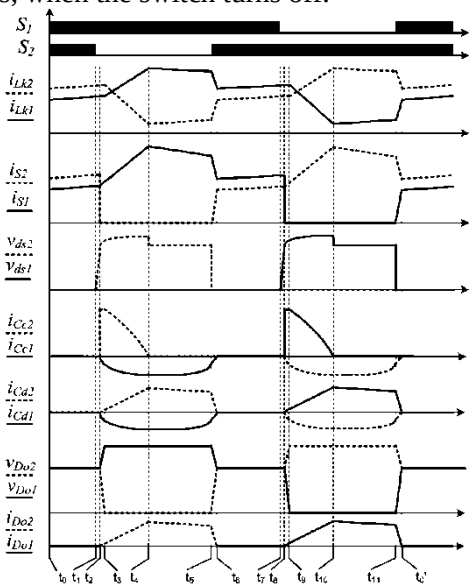

Figure.3.Waveform of proposed converter

Operational Principles: The WCCI can be modeled as the combination of a magnetizing inductor, an ideal transformer with corresponding turns ratio and the leakage inductances in each winding. The equivalent circuit of the proposed converter is shown in Fig. 4, where $Lm1$, $Lm2$ are the magnetizing inductors; L_{Lka}, L_{Lkb} are the leakage inductances in the primary winding of each WCCI; L_{Lkc} is the summation leakage inductance of the second

winding of WCCI 1 and the third winding of WCCI 2; L_{Lkd} is the summation leak- age inductances of the second winding of WCCI 2 and the third winding of WCCI 1; *Dc*1 and *Dc*2 are the clamp diodes; *Cc*1 and *Cc*2 are the clamp capacitors; *Dr*1 and *Dr*2 are the regenerative diodes; *Cd*1 and *Cd*2 are the series capacitors; *S*1 and *S*2 are the power switches; *Do*1 and *Do*2 are the output diodes; *Co* is the output capacitor. V_{in} and V_{out} are the input and output voltages. *N* is defined as the turn's ratio $n2/n1$.

The key steady state waveforms of the proposed converter are shown in Fig. 3. There are 12 stages in one switching period. Due to the symmetry of the circuit, only six stages are analyzed here and the corresponding equivalent circuits for each operational stage are shown in Fig. 4.

Stage 1 [t_0- t_1]: The switches S_1 and S_2 are both in turn on state before t_1. The output diodes D_{o1} and D_{o2} are both reverse-biased. The diodes D_{c1}, D_{c2}, D_{r1} and D_{r2} are all in turn-off state. The magnetizing inductors L_{m1}, L_{m2} and the primary leakage inductances L_{LKA}, L_{LKB} are charged linearly by the input voltage.

$$\mathbf{i_{Lm1}(t) = I_{Lm1}(t_0) + \frac{V_{in}}{L_{m1} + L_{Lka}} t} \quad (1)$$

$$\mathbf{i_{Lm2}(t) = I_{Lm2}(t_0) + \frac{V_{in}}{L_{m2} + L_{Lkb}} t} \quad (2)$$

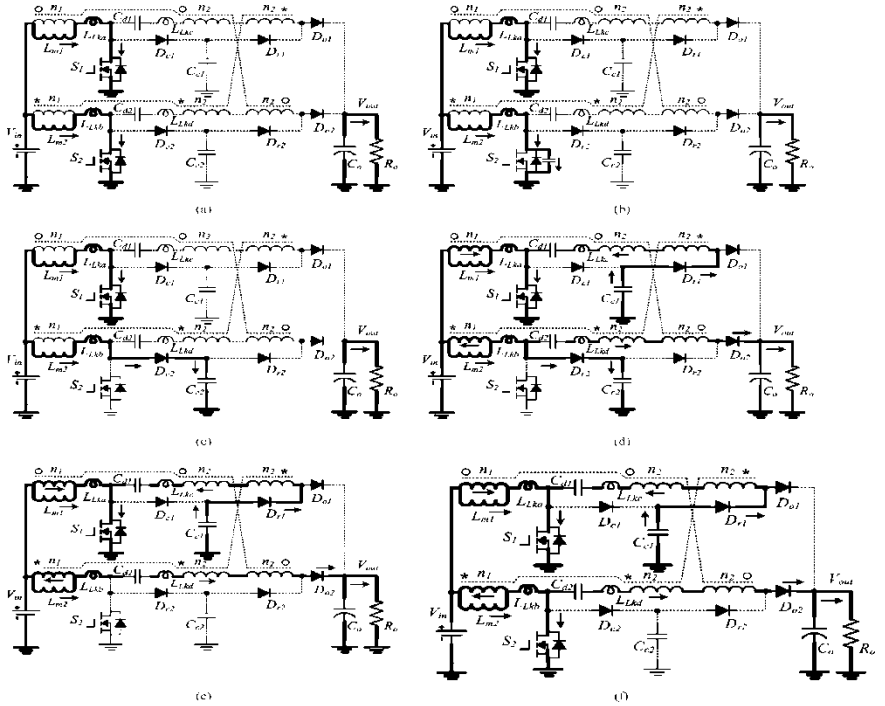

Figure.4.Operation stages of the proposed converter. (a) Stage 1 [*t*0 –*t*1]; (b) Stage 2 [*t*1 –*t*2]; (c) Stage 3[*t*2 –*t*3]; (d) Stage 4 [*t*3 –*t*4]; (e) Stage 5 [*t*4 –*t*5]; (f) Stage 6 [*t*5 –*t*6].

Stage 2 [t_1- t_2]: At t1, the switch S_2 turns off. The parasitic drain-source capacitor C_{S2} of S_2 is charged by the current of the magnetizing inductor L_{m2} in an approximately linear way. The voltage of the clamp diode D_{c2} decreases as the drain-source voltage of S_2 increases. This stage is very short due to the small capacitance of C_{S2}

$$\mathbf{V_{ds2}(t) = \frac{I_{Lm2(t_1)}}{C_{S2}} t} \quad (3)$$

Stage 3 [t_2, t_3]: At t_2, the voltage of the clamp diode D_{c2} decreases to zero and it begins to conduct. The clamp capacitor C_{c2} is charged by the current of the magnetizing inductor L_{m2} linearly. The switch S_2 turns off and its drain-source voltage v_{ds2} is clamped by the capacitor C_{c2}. The energy stored in the leakage inductance L_{Lkb} starts to transfer to the C_{c2}

$$\mathbf{V_{ds2}(t) = V_{ds2}(t_2) + \frac{I_{Lm2(t_2)}}{C_{S2}} t} \quad (4)$$

Stage 4 [t_3- t_4]: At t_3, the voltage of D_{o2} decreases to zero and it begins to turn on. The current increasing rate through D_{o2} is determined by the leakage inductance L_{Lkd}. As the current through D_{o2} increases, the current through the C_{c2} decreases. The series capacitor C_{d2}, the second winding of WCCI 2 and the third winding of WCCI 1 operate as voltage sources, which is in series to extend the voltage gain. Meanwhile, due to the transformer function of the coupled inductor, the regenerative diode Dr1 begins to conduct. The energy stored in C_c1 starts to transfer to C_{d1} through Dr1, the second winding of WCCI 1 and third winding of WCCI 2 and the switch S1. The current throughCc1 andCd1 is controlled by the leakage inductance L_{Lkc}. The current expression can be derived by

$$\mathbf{i_{S1}(t) = i_{Lm1}(t) + (N+1)i_{Dr1}(t) + Ni_{Do2}(t)} \quad (5)$$

$$\mathbf{i_{Cc2}(t) = i_{Lm2}(t) + Ni_{Dr1}(t) - (N+1)i_{Do2}(t)} \quad (6)$$

$$\mathbf{i_{Lkb}(t) = i_{Cc2}(t) + i_{Do2}(t)} \quad (7)$$

Stage 5 [t_4- t_5]: At t_4, the current through the clamp capacitor C_{c2} decreases to zero and the clamp diode D_{c2} turns off naturally. There is no reverse-recovery problem for the clamp diodes. The energy stored in the series capacitor C_{d2} continues to transfer to the load. The current through D_{o2} is determined by the leakage inductances L_{Lkb} and L_{Lkd}.

Stage 6 [t_5- t_6]: At t_5, the switch S_2 turns on. Due to the leakage inductance L_{Lkb}, S_2 turns on with ZCS soft switching condition. The leakage inductance L_{Lkb} is quickly charged by the summation of the input voltage, the voltage on the series capacitor C_{d2}, the reflected voltages of the second winding of WCCI 2 and the third winding of WCCI 1. The current falling rate through D_{o2} is controlled by the leakage inductance L_{Lkd} , which alleviates the output diode reverse recovery problem. This stage ends when the output diode D_{o2} turns off

$$\mathbf{i_{Do2}(t) \approx I_{Do2}(t_5) - \frac{V_{out}-V_{cd2}}{L_{Lkd}}\, t} \quad (8)$$

Converter Performance Analysis: Due to the circuit symmetry of the proposed converter, it is reasonable to consider $Lm1 = Lm2 = Lm$, $Cc1 = Cc2 = Cc$, $Cd1 = Cd2 = Cd$. In order to simplify the analysis, the leakage inductance is assumed to be zero and the voltages on the clamp capacitor Cc and the series capacitor Cd is considered to be constant during the whole switching transition. The detailed performance of the presented converter is analyzed as follows.

Voltage Gain Expression: From the steady analysis in the above section, the charging voltage of the magnetizing inductor Lm is the input voltage Vin during the switch turn-on stage and the discharging voltage during the switch turn-off stage is given by

$$\mathbf{V_{Lm\_dis} = \frac{V_{out}-2(N+1)V_{in}}{2(N+)}} \quad (9)$$

By applying the voltage-second balance to the magnetizing inductor, the output voltage gain is given by

$$\boldsymbol{M = \frac{V_{out}}{V_{in}} = \frac{2(N+1)}{1-D}} \quad (10)$$

where M is the voltage gain, N is the turns ratio of the WCCIs and D is duty cycle of the switch. From (10), it is clear that the proposed converter can achieve a high voltage gain because another two parameters appear in the numerator compared with the conventional boost converter. The detailed curve of the voltage gain M related to the turns ratio N and the duty cycle D is given in Fig. 5. As

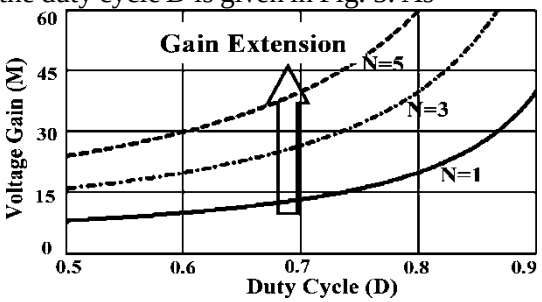

Figure.5. Voltage gain curve versus turns ratio and duty cycle

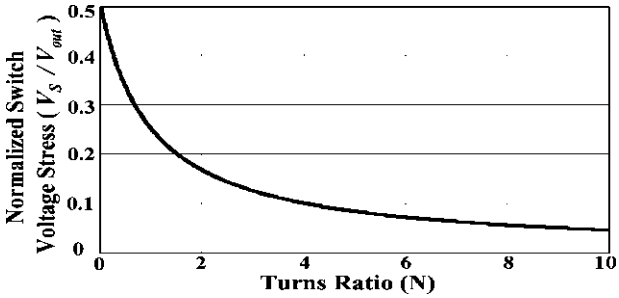

Figure.6.Plot of normalized switch voltage stress versus turns ratio

The duty cycle and the turns ratio increase, the voltage gain increases greatly, which makes the proposed converter able to avoid the extreme duty cycle and the large peak current existed in the conventional boost converter in high step-up applications.

The voltage multiplier cells are in series to the power branch to double the voltage gain under the same turns ratio and duty cycle condition compared with the interleaved high step-up converters published in [13-[15] with only WCCI's.

Voltage Stress Analysis: The voltage ripple on the clamp capacitors and the series capacitors are ignored to simplify the voltage stress analysis on the components of the proposed converter. The voltage stress of the clamp capacitors Cc 1 and $Cc2$ is given by

$$\mathbf{V_{Cc} = \frac{V_{in}}{1-D} = \frac{V_{out}}{2(N+1)}} \quad (11)$$

The voltage stresses of the switches $S1, S2$ and the clamp diodes $Dc1, Dc2$ are equal to that of the clamp capacitors, which are given by

$$\mathbf{V_s = V_{Dc} = V_{Cc} = \frac{V_{in}}{1-D} = \frac{V_{out}}{2(N+1)}} \quad (12)$$

The switch voltage stress is determined by the turns ratio of the WCCIs. The curve of the normalized switch voltage

stress as a function of the turns ratio of the WCCIs is plotted in Fig. 6 It is shown that the maximum switch voltage stress is half of the output voltage. As the turn ratio increases the switch voltage stress decreases, which makes it possible that low-voltage power MOSFETs with low $R_{DS\ ON}$ can be employed in high step-up and high output voltage applications. As a result, the conduction losses are reduced compared with the conventional boost converter. The voltage stress of the series capacitors $Cd1$ and $Cd2$ is given by

$$\mathbf{V_{Cd} = V_{out} - (N+1)V_{in} = \frac{(N+1)(1+D)}{1-D} V_{in}} \quad (13)$$

The voltage stress of the output diodes $Do1$ and Do2 can be derived

$$\mathbf{V_{Do} = V_{out} - V_{Cc} = \frac{2N+1}{1-D} V_{in} = \frac{2N+1}{2(N+1)} V_{out}} \quad (14)$$

The output diode voltage stress increases as the turns ratio increases, but it is always lower than the output voltage. The minimum voltage stress of the output diode is half of the output voltage.

The voltage stress of the regenerative diode D_{r1} and D_{r2} can be derived by

$$\mathbf{V_{Dr} = V_{out} - V_{Cc} = \frac{2N+1}{1-D} V_{in} = \frac{2N+1}{2(N+1)} V_{out}} \quad (15)$$

It can be seen that the voltage stress of the regenerative diodes is same as that of the output diodes.

Soft Switching Performance: Due to the leakage inductance of the WCCIs, ZCS turn-on is realized for the switch $S1$ and $S2$, which reduces the switching losses. When the switch turns off, the leakage energy is transferred to the clamp capacitor through the clamp diode, which absorbs the voltage spikes on the MOSFETs and recycles the leakage energy. Furthermore, the output diode current falling rate is controlled by the leakage inductance existed in the second and the third windings of the WCCIs, which improves the output diode reverse-recovery problem and reduces the reverse- recovery losses. The clamp diode turns off naturally, so there is no reverse-recovery problem for the clamp diode

Cc and Cd Design Consideration: The voltage ripple on the capacitors Cc and Cd is the main consideration for the capacitor design. From the steady operational analysis, it can be derived that the variation of the electric charge on the capacitors Cc and Cd is the electric charge transferred to the load in each switching period. The relationship between the voltage ripple and the output power can be derived by

$$\mathbf{C = \frac{P_{out}}{2f_s V_{out} \Delta V_c}} \quad (16)$$

Where P_{out} is power output, f_s is the switching frequency, V_{out} is the output voltage and ΔVc is the voltage ripple on the capacitor Cc or Cd. It can be seen that the voltage ripple can be reduced when a large capacitor is employed. However, the large capacitor is bulky and costly. The design of the capacitors Cc and Cd should make a compromise between the voltage ripple cancellation and the cost.

Limitation of the Turns Ratio: From the steady operational analysis, it can be concluded that the duty cycle of the proposed converter should be exceeded 0.5. So the limitation of the turns ratio can be derived by

$$\mathbf{N \leq \frac{V_{out}}{4V_{in}} - 1} \quad (17)$$

3. SIMULATED RESULTS

In order to verify the effectiveness of the proposed converter, the simulation is done as follows: V_{in}: 40 V; converter output voltage V_{out}: 404 V; converter output power Pout: 1kW; inverter output voltage: 418V; inverter output current 10A; supply frequency: 50Hz; n2/n1: 20/25; Lm : 95 μH; Co : 470 μF; $Cc1$ and $Cc2$: 2.2 μF; $Cd1$ and $Cd2$: 4.7 μF; R_o: 145ohms. Solar cell converts sunlight into electricity, using the process of photovoltaic effect. One silicon solar cell produces 0.5 Volt. Here a 40 V PV output is shown in Fig. 7

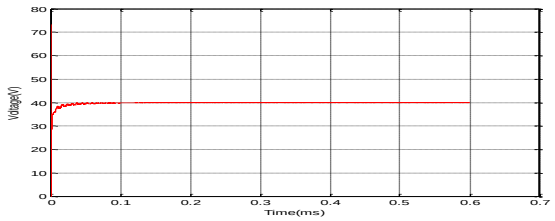

Figure.7. PV Output Voltage

The simulated results for switch gate signals and the drain source voltage of S1 and S2 is shown in Fig. 8. It can be seen that the gate signals are interleaved to reduce the current ripple and to increase the power level. The switch voltage stress is about 100V. So, low voltage MOSFET is available here to reduce the conduction losses in high step-up and high-output voltage applications.

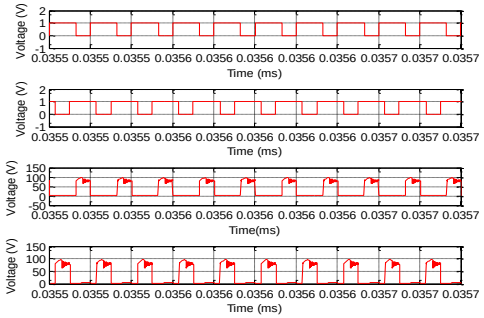

Figure.8. Gate Voltage & Switch Voltage Across S1 & S2

The output of the converter is boosted up to 404 V with a gain of 10.2 with a duty cycle of 54% at N=1.3, this is achieved due to interleaved converters with voltage multiplier cells and WCCI. The output voltage and power of converter is shown in Fig. 9 and Fig. 10 respectively

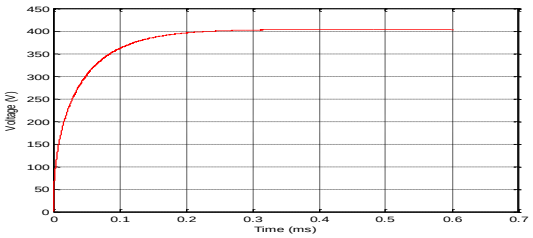

Figure.9. Converter Output Voltage

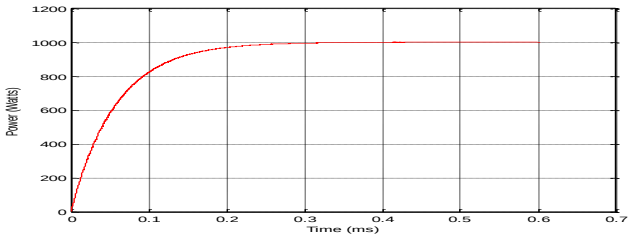

Figure.10.Output Power of Converter

A three phase inverter is simulated using PWM technique. Here a sinusoidal PWM waveform is shown in Fig. 11. In this method of modulation, several pulses per half cycle are used. In SPWM, the pulse width is a sinusoidal function of angular position of pulse in a cycle.

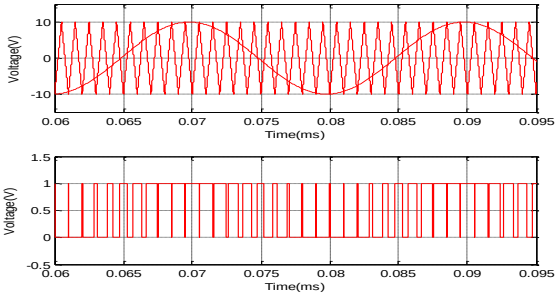

Figure.11.PWM Pulse for three phase inverter

The inverter output voltage for V_{ab} is shown in Fig. 12. Here we get an output voltage of 418V from a single phase inverter using sinusoidal PWM technique. The output from the inverter is fed to an asynchronous motor.

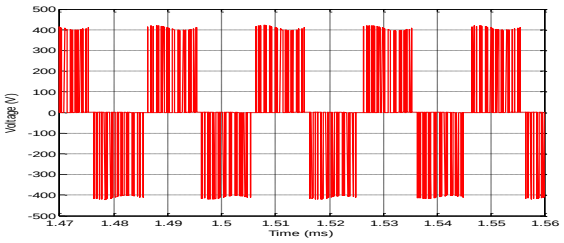

Figure.12.Inverter Output Voltage

4. CONCLUSION

An interleaved boost converter integrated with WCCIs and voltage multiplier cells was introduced in this paper. The voltage gain is extended and the extreme duty cycle is avoided by the WCCIs and the voltage multiplier cells compared with the conventional interleaved boost converter, which can reduce the peak current and voltage stress on the switches to reduce the conduction losses. Moreover, ZCS turn-on for the switch is achieved and the output diode reverse recovery problem is relieved by the leakage inductance to reduce the switching losses and EMI noises. Furthermore, the leakage energy is recycled and the volt- age spikes on the power MOSFETs are absorbed by the voltage multiplier cells. The simulated and experimental results showed that the proposed converter is a suitable topology candidate for high step-up, high power applications.

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